Arm Accredited Engineer

1. Within the ARMv7 architecture, which one of the following features is unique to the ARMv7-A profile?

A. Privileged execution

B. Virtual memory support

C. Cache support

D. The ARM instruction set

Answer(s): B

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2. In an ARMv7-A processor that includes the Advanced SIMD extension (NEON), where are the data values operated on by NEON instructions stored?

A. In registers shared with the VFP register set

B. In dedicated registers not shared with other registers

C. In registers shared with the integer register set

D. In system memory

Answer(s): A

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3. A re-entrant interrupt handler would typically be used to:

A. Reduce response time for higher priority interrupts

B. Allow an interrupt handler to be relocated in memory

C. Avoid the need for an interrupt handler to use a stack.

D. Allow an external interrupt to interrupt an SVC handler

Answer(s): A

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4. A program running on a development board that is connected to a host using a debugger can access a file on the host by using:

A. Semihosting

B. Virtual I/O

C. Polling

D. Memory mapping

Answer(s): A

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5. Which TWO of the following accurately describe constraints on the location of the Tightly Coupled Memory (TCM) regions in a Cortex-R4 processor? (Choose two)

A. TCM Region B (BTCM) must be located immediately above TCM Region A (ATCM)

B. Both TCM regions must be placed at addresses which are aligned to their size

C. TCM Region A (ATCM) must be at a lower memory address than TCM Region B (BTCM)

D. TCM Region A can only be located at address 0x0

E. The two TCM regions may not overlap

Answer(s): B

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6. Assume a Big-Endian (BE) memory system with the following memory contents.

A. 0x22114433

B. 0x44332211

C. 0x11223344

D. 0x33441122

Answer(s): C

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7. In which TWO of the following locations would a compiler typically place local variables? (Choose two)

A. ROM

B. Stack

C. Registers

D. Cache

E. Heap

Answer(s): B,C

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8. In the Generic Interrupt Controller (GIC) architecture, which of the following ID numbers are reserved for interrupts that are private to a CPU interface?

A. ID0-ID63

B. ID0-ID31

C. ID0-ID7

D. ID0-ID15

Answer(s): B

9. Which of these instructions is a correct translation of the body of function f?

A. LDR r0, [r0], #1

B. LDR r0, [r0]. #4

C. LDR r0, [r0.#1]

D. LDR r0, [r0. #4]

Answer(s): D

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10. Which one of the following features must any processor support to conform to the ARMv7-A architecture?

A. Thumb-2 technology

B. TrustZone (Security Extensions)

C. NEON (Advanced SIMD)

D. Generic Interrupt Controller

Answer(s): A

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11. What architecture does the ARM11 MPCore implement?

A. ARMv7-A with the Multiprocessing Extensions

B. ARMv6

C. ARMv7-A

D. ARMv6K

Answer(s): D

12. Processors which implement the ARMv7-A architecture can be configured to allow unaligned memory access. Unaligned accesses have a number of advantages, disadvantages, and limitations.

A. Unaligned accesses may take more cycles to execute than aligned accesses

B. Unaligned accesses can only be made to Normal memory

C. If the relevant control register setting is enabled all loads and stores can function from unaligned addresses

D. A program compiled using unaligned accesses can be safely executed on all ARMv7-A devices

E. Unaligned loads and stores are necessary for accessing fields in packed structures

Answer(s): A,B

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13. The Memory Protection Unit (MPU) of Cortex-R4 performs which of the following tasks?

A. Generates parity information to detect soft errors in memory

B. Permits the system to be divided into secure and normal worlds, through the use of ARM's TrustZone technology

C. Performs access permission checks

D. Translates virtual addresses to physical addresses

Answer(s): C

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14. Which of the following is a REQUIRED feature in the ARMv7 architecture?

A. A memory management unit

B. The Thumb-2 instruction set

C. Integer division instructions

D. NEON

Answer(s): B

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15. Under which of the following data-sharing scenarios would cache maintenance operations be necessary?

A. Sharing data with another thread running on the same core

B. Sharing data with another CPU in an SMP system

C. Sharing data with another process running on the same core

D. Sharing data with an external device

Answer(s): D

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16. Using a Generic Interrupt Controller (GIC), when the interrupt handler writes to the End of Interrupt Register (ICCEOIR), which of the following state transitions might occur for that interrupt ID?

A. Active to Pending

B. Inactive to Active

C. Active to Inactive

D. Pending to Active

Answer(s): C

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17. A deeply embedded real-time industrial control system is missing some hard real-time interrupt deadlines. Which of the following performance analysis techniques is the most suitable for identifying which routines are causing the problem?

A. Use an ETM instruction trace profiler, which outputs information about the program as it runs

B. Use a JTAG sample-based profiler, which periodically halts the CPU, and dumps information about the interrupted process

C. Add some serial logging to the software, which outputs information about the program as it runs

D. Add a new interrupt handler, which is triggered off a timer, and dump information about the interrupted process

Answer(s): A

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18. An ARMv7 implementation might include the VFPv4-D32 floating point extension. What does the '32' indicate?

A. The number of bits of data that can be loaded or stored at once

B. The number of integer operations that can be performed simultaneously

C. The number of double precision floating point registers implemented

D. The width of the datapath in bits

Answer(s): C

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19. In which of the following situations would you use a mutex to avoid synchronization problems?

A. Two independent threads running on a single processor both need to access a single UART

B. In a dual-core system, a UART is accessed by a single thread running on one of the processors

C. A single-threaded application needs to manage two separate UART peripherals

D. In a dual-core system, processor A needs to access UART A and processor B needs to access UART B

Answer(s): A

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20. According to the EABI. what would the C size of () operator return when given the following structure?

A. 24

B. 19

C. 20

D. 28

Answer(s): A
